What is claimed is:

1. A ferroelectric memory device, comprising:

a semiconductor substrate providing elements of a transistor;

a first inter-layer insulating layer formed on the semiconductor substrate;

a storage node contact connected to elements of the transistor by passing through the first inter-layer insulating layer;

a barrier layer contacting simultaneously to the storage node contact and the first inter-layer insulating layer;

a lower electrode having a space for isolating the first inter-layer insulating layer and being formed on the barrier layer;

a glue layer being formed on the first inter-layer insulating layer and encompassing lateral sides of the lower electrode as filling the space;

a second inter-layer insulating layer exposing a surface of the lower electrode and encompassing the glue layer;

a ferroelectric layer formed on the glue layer including the second inter-layer insulating layer; and

an upper electrode formed on the ferroelectric layer.

2. The ferroelectric memory device as recited in claim 1, wherein the storage node contact has the identical planar level to a surface of the first inter-layer insulating layer,

and the barrier layer is formed in a single layer on the storage node contact.

3. The ferroelectric memory device as recited in claim 1, wherein a height of the storage node contact is different from that of the first inter-layer insulating layer, and the barrier layer includes a first barrier layer having the identical planar level to the first inter-layer insulating layer surface as being filled into a portion formed by the above height difference and a second barrier layer contacting to the first inter-layer insulating layer by being formed on the first barrier layer.

4. The ferroelectric memory device as recited in claim 1, wherein a thickness of the glue layer for filling the space is identical to that of a portion encompassing the lower electrode and that of the glue layer formed on the first inter-layer insulating layer.

5. The ferroelectric memory device as recited in claim 1, wherein the glue layer is made of any one material or more than one material selected from a group consisting of Al_2O_3, ZrO_2, HfO_2, Bi_2O_3, Ta_2O_5, TiO_2 and silicon nitride.

6. The ferroelectric memory device as recited in claim 1, wherein the storage node contact is either a tungsten plug or a polysilicon plug.

7. The ferroelectric memory device as recited in claim 1, wherein the lower electrode has a wider area than that of the barrier layer.

8. A method for fabricating a ferroelectric memory device, comprising the steps of:

forming a storage node contact making a contact to a semiconductor substrate by passing through the first inter-layer insulating layer formed on the semiconductor substrate;

forming a stack pattern of a barrier layer connected to the storage node contact and a lower electrode;

forming a space between the lower electrode and the first inter-layer insulating layer by removing selectively lateral sides of the barrier layer;

forming simultaneously a glue layer encompassing the lateral sides of the lower electrode as filling the space;

forming a second inter-layer insulating layer exposing a surface of the lower electrode as laterally encompassing the glue layer;

forming a ferroelectric layer on the second inter-layer insulating layer including the lower electrode; and

forming an upper electrode on the ferroelectric layer.

9. The method as recited in claim 8, wherein the step of forming the storage node contact includes the steps of:

forming a storage node contact hole exposing a partial portion of the semiconductor substrate by etching the first

inter-layer insulating layer;

depositing a plug layer on the first inter-layer insulating layer having the storage node contact hole;

forming the storage node contact plug of which partial portion is filled into the storage node contact hole through a recess etch-back process performed to the plug layer;

depositing a second barrier layer on the first inter-layer insulating layer having the storage node contact plug; and

planarizing the second barrier layer through a chemical mechanical polishing process to thereby have the same surface level to that of the first inter-layer insulation layer.

10. The method as recited in claim 9, wherein the step of forming the stack pattern of the barrier layer includes the steps of:

depositing the first barrier layer on the first inter-layer insulating layer having the second barrier layer;

forming a conductive layer for forming the lower electrode on the second barrier layer;

forming a mask defining the lower electrode on the conductive layer; and

forming the stack pattern of the first barrier layer and the lower electrode by etching the conductive layer and the second barrier layer with use of the mask as an etch mask.

11. The method as recited in claim 10, wherein the first

barrier layer is subjected to an etch-back process or a chemical mechanical polishing process before forming the conductive layer.

12. The method as recited in claim 8, wherein, at the step of forming the space between the lower electrode and the first inter-layer insulating layer, a wet type etching process using a solution capable of selectively dissolving the first barrier layer is performed.

13. The method as recited in claim 12, wherein the etch solution uses at least more than one solution selected from a group consisting of H_2SO_4, HNO_3 and H_3PO_4, or uses a mixed solution obtained by adding H_2O_2 or NH_4OH to the above selected solution.

14. The method as recited in claim 8, wherein the step of forming simultaneously the glue layer and the second inter-layer insulating layer includes further the steps of:

forming the glue layer on the lower electrode and the first inter-layer insulation layer until having a thickness to fill the space;

forming the second inter-layer insulating layer on the glue layer; and

planarizing the second inter-layer insulating layer and the glue layer until exposing a surface of the lower electrode.

15. The method as recited in claim 14, wherein at the step of planarizing the second inter-layer insulating layer and the glue layer, the second inter-layer insulating layer and the glue layer are subjected to a chemical mechanical polishing process all at once, or the second inter-layer insulating layer is firstly proceeded with a chemical mechanical polishing process followed by an etch-back process performed to the exposed glue layer thereafter.

16. The method as recited in claim 8, wherein the step of forming the storage node contact includes the steps of:

forming a storage node contact hole exposing a partial portion of the semiconductor substrate by etching the first inter-layer insulating layer;

depositing a plug layer on the first inter-layer insulating layer having the storage node contact hole; and

forming the storage node contact plug completely filled into the storage node contact hole through a recess etch-back process performed to the plug layer.

17. The method as recited in claim 16, wherein the step of forming the stack pattern of the barrier layer includes the steps of:

depositing the barrier layer on the first inter-layer insulating layer having the storage node contact hole;

forming a conductive layer for forming the lower electrode on the barrier layer;

forming a mask defining the lower electrode on the conductive layer; and

forming the stack pattern of the barrier layer and the lower electrode by etching the conductive layer and the barrier layer with use of the mask as an etch mask.

18. The method as recited in claim 8, wherein the glue layer is made of any one material or more than one material selected from a group consisting of Al_2O_3, ZrO_2, HfO_2, Bi_2O_3, Ta_2O_5, TiO_2 and silicon nitride.